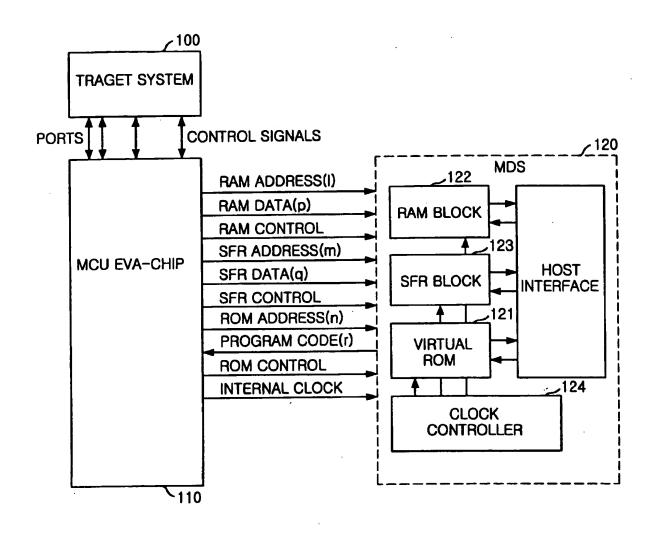
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DEVELOPMENT SYSTEM FIG. 1

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FIG. 1 <PRIOR ART>



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FIGS. 2 and 3

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FIG. 2

PORT0	PCL	PCL	RAMADDR	
PORT1	PCH	PCH	SFRDB	
PORT2.7 (RAM_WEB)				

FIG. 3

PORT0	PCL	PCL	SFRAB	
PORT1	PCH	PCH	SFRDB	
PORT2.6 (SFR_WEB)				

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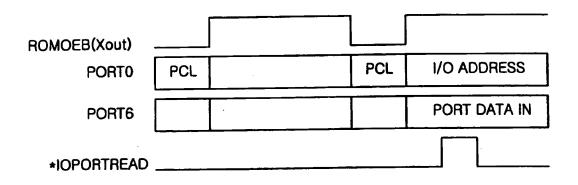
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FIG. 4



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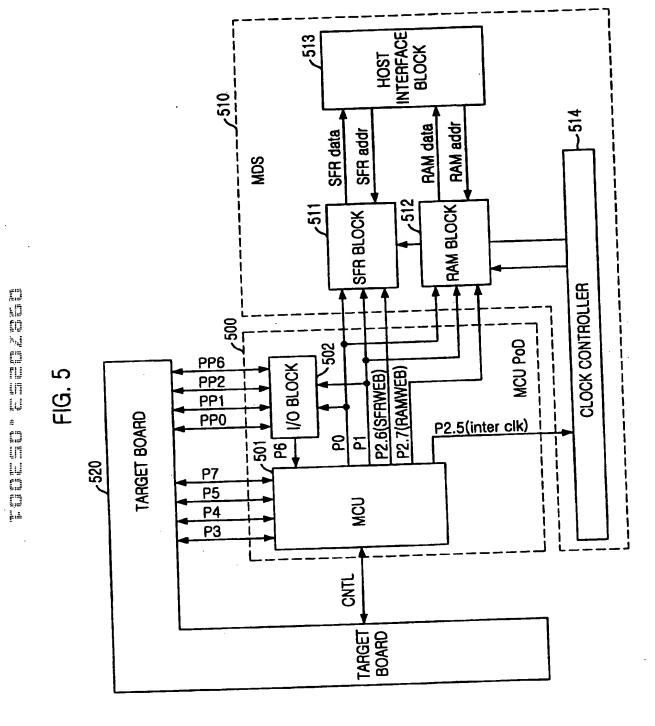
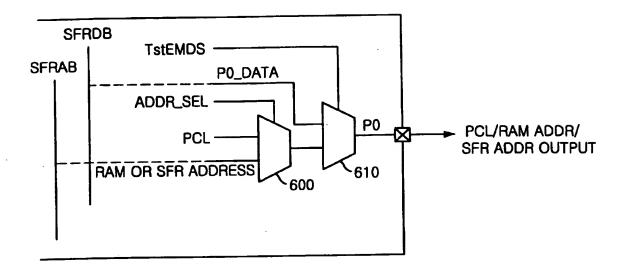


FIG. 6



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DEVELOPMENT SYSTEM FIG. 7

FIG. 7

